ASDQ++ Front-end board for the MWPC readout of the LHCb Muon System

LHCb Technical Note

Issue: 1

Revision: 1

Reference: LHCb 2002-014 Muon
Created: 25 December 2001
Last modified: 25 April 2002

Prepared by: G.Chiodi[1], G.Corradi[2], G.Felici[2], M.Gatta[2], A. Kashchuk[3, 4], B.Schmidt[3]
[1] *University of Rome, 'La Sapienza' and INFN, Italy*
[2] *LNF, Frascati, INFN, Italy*
[3] *CERN, 1211 Geneva 23, Switzerland*
[4] *PNPI, Gatchina, Russia*
Corresponding author: Anatoli.Kachtchouk@cern.ch

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Revision: 1
Issue: 1
Last modified: 25 April 2002

Abstract

Schematics of both the 16-channel Spark Protection Board (SPB) and the 16-channel Amplifier Chip Board (ACB) based on the ASDQ chip are presented. The boards are used for the readout of wire strips and cathode pads of the MWPC prototypes, designed and tested for the Muon System of the LHCb experiment. The post-radiation measurements made at CERN indicate suitable operation of both boards up to doses of 3 *MRad* and 1×10^{14} *protons/cm*^{2} at *24GeV/c*.

Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Method for test and diagnostics of the on-detector FEE during experiment **2. Document Reference Number: LHCb 2002-014**			
3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
1	1	25 April 2002	First version

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1 Introduction

Multi-Wire-Proportional-Chambers (MWPC) with a wire pitch of 1.5 mm and 5 mm gas gap will be used in muon stations for a large part of the LHCb Muon System [1]. Depending on the chamber position in the system, the chambers have either anode wire or cathode pad or a combined readout. The detector capacitance ranges from 20 pF to 200 pF throughout the system. The expected rate ranges from about 100*Hz* to 1*MHz* per channel.

Each muon station is required to have an efficiency >99% in a time window of 20 ns. In order to achieve this, a logical OR of two independent double gaps is foreseen in each muon station.

According to the LHCb Muon TDR [1], the system is composed of 120,000 physical channels and 26,000 logical channels, which are sent to the L0 muon trigger and the DAQ. The new ASIC (CARIOCA) under development at CERN is considered as a baseline FE-chip for the LHCb Muon System. It is designed in the 0.25μm CMOS radiation tolerant technology of IBM. The ASDQ chip developed at University of Pennsylvania [2] is considered as backup solution and has been tested extensively in test beams [3-5].

The 16-channel Amplifier Chip Board (ACB) presented here is based on the ASDQ chip and was designed and used for beam tests of the MWPC prototypes constructed at CERN and LNF. The 16-channel Spark Protection Board (SPB) is a separate board located in front of the ACB in order to protect it from possible sparks. Full schematics as well as the layout of both 16-channel boards, ACB and SPB, are presented in this technical note.

The layout of the boards can be considered as a general solution, i.e. the front-end electronics (FEE) boards based on CARIOCA will be compatible to the ACB based on the ASDQ and use the same SPB as presented below.

The goal of this note is to show how the boards have been made. Some important characteristics of the front-end electronics based on the ASDQ++ can be found in Ref. [3-5].

2 ASDQ++ conception

The ASDQ chip [2] has many nice features, but very limited range of detector capacitance and rather high input impedance.

The simple modification shown in Fig.1 avoids both disadvantages. A common base transistor connected either to input *InA* of the ASDQ chip (in case of wire read-out) or *InB* (in case of cathode read-out) drastically improves the system. The input impedance can be reduced by an order of magnitude and is constant in a wide frequency range ($R_{in}=25\Omega$ *at* $I_E=1mA$). The detector capacitance can be extended by an order of magnitude with this configuration. Both features are achieved without disturbance of the main characteristics of the ASDQ chip, i.e. its good performance at high rates, excellent pulse shaping and other features. We refer to the modified version as ASDQ++ [3]. The equivalent noise charge (ENC) for the ASDQ++ is 1440+37e^-/pF, compared to 1190+70e^-/pF, measured for the ASDQ chip itself [2].

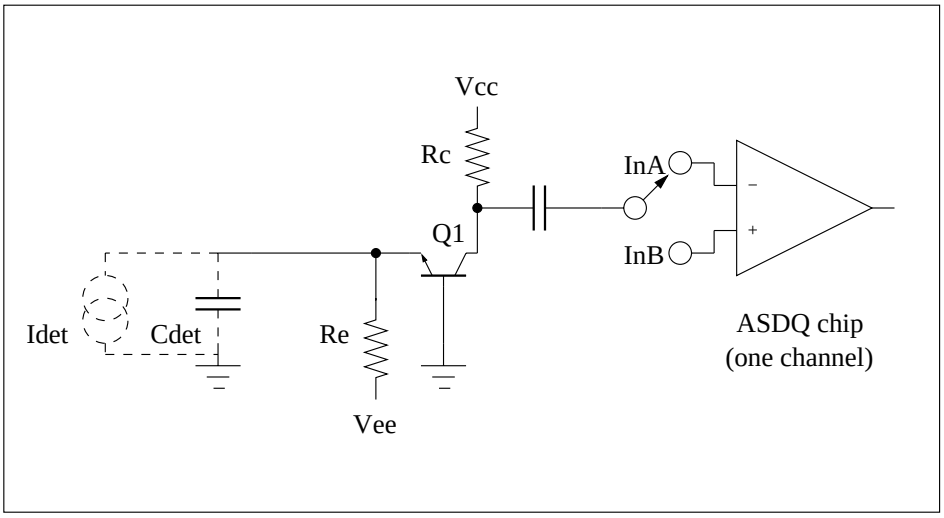

Fig.1. The modified ASDQ++ schematics. A common base transistor connected either to input InA of the ASDQ chip (in case of wire read-out) or InB (in case of cathode read-out) drastically improves the system. The input impedance can be reduced by an order of magnitude. The detector capacitance can be extended by an order of magnitude.

One additional problem of the ASDQ chip has been found during our tests. It has to do with the configuration of the *BLR* and leads to an increase in cross talk in case of wire strip readout [4].

3 16-channel Amplifier Chip Board

The schematics and layout of the 16-channel Amplifier Chip Board (ACB) based on the ASDQ++ conception are presented in Fig.2 to 4. The board consists of two ASDQ chips. One chip will receive signals from 8 channels of the first double gap MWPC and the second one from the second double gap (cf. [1], Fig.46 to 48). The ASDQ pad definitions referred to in the following paragraphs are explained in Appendix A.

The transistor used in front of each ASDQ channel is the Philips BFR93A (Q1 in Fig.1). The ±3V applied to the ACB limit the choice of resistors in both collector and emitter of the front-end transistor. The resistor R_E=2.2kΩ provides I_E≈1mA in case of the 3V power supply. Other components have values of R_C=1.6kΩ and C=100nF (Fig.2). However, there is also an option to assemble the ACB with separated voltages for the first transistor and the chip, in order to improve the signal-to-noise ratio (for example, ±12V and R_E=11kΩ, which will provide I_E≈1mA and reduces the parallel noise to ENC_p=1100e^-).

We use fixed bias voltages for the following ASDQ chip inputs: ID (+3V), IBLRM (+3V), QDR (-3V), QEN (+3V), IBLR (+1.5V for cathode readout, -0.7V for wire readout). It is done by the corresponding voltage dividers. We provide voltage variations, as mentioned in brackets, for the chip inputs: DTHR (in range from zero to +1V), TREFE (-3V/+1.5V), TREFO (-3V/+1.5V). There is one digital TTL level to control ATT. In order to control ACB we used the controller designed as a NIM module.

DTHR is the common threshold for all channels. There are test points (ST1, cf. Fig. 2) in order to measure the threshold directly on the chip.

ATT introduces in each channel the gain attenuation by factor 2 (if enabled).

The ACB printed circuit board is the same for both negative and positive input signal polarities. However, the assembling of the board differs for the two polarities. A network with zero resistors located close to inputs of the ASDQ chip specifies the needed polarity.

16 outputs compatible to LVDS (Low Voltage Differential Signal, +1.3V offset voltage and 2mA current) are sent from the ACB to be recorded by the Data Acquisition System (DAQ). Each output has two pull-up 1kΩ resistors connected to +3V.

The ASDQ chip has differential analog outputs from channel 8 for monitoring (cf. BLA and BLB in Fig.2). It has also differential test inputs (TSTN and TSTP), through which the strobe pulse (10ns in width) is sent to the chip. This strobe injects test charges in each channel of the chip. The charge value depends of the voltages on TREFE and TREFO inputs. To use this facility we set on the ACB additional connectors. An additional board (not presented here) connected to these connectors is used for tests of the ACB. This board can test separately either even or odd channels of the ASDQ chip.

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It must be noted, that there are two ‘grounds’ (GND) on the board: one is incoming ground D or digital one, and the second is analog ground A. As shown in Fig.2, the small resistor (about 3.3Ω) is set between the grounds D and A.

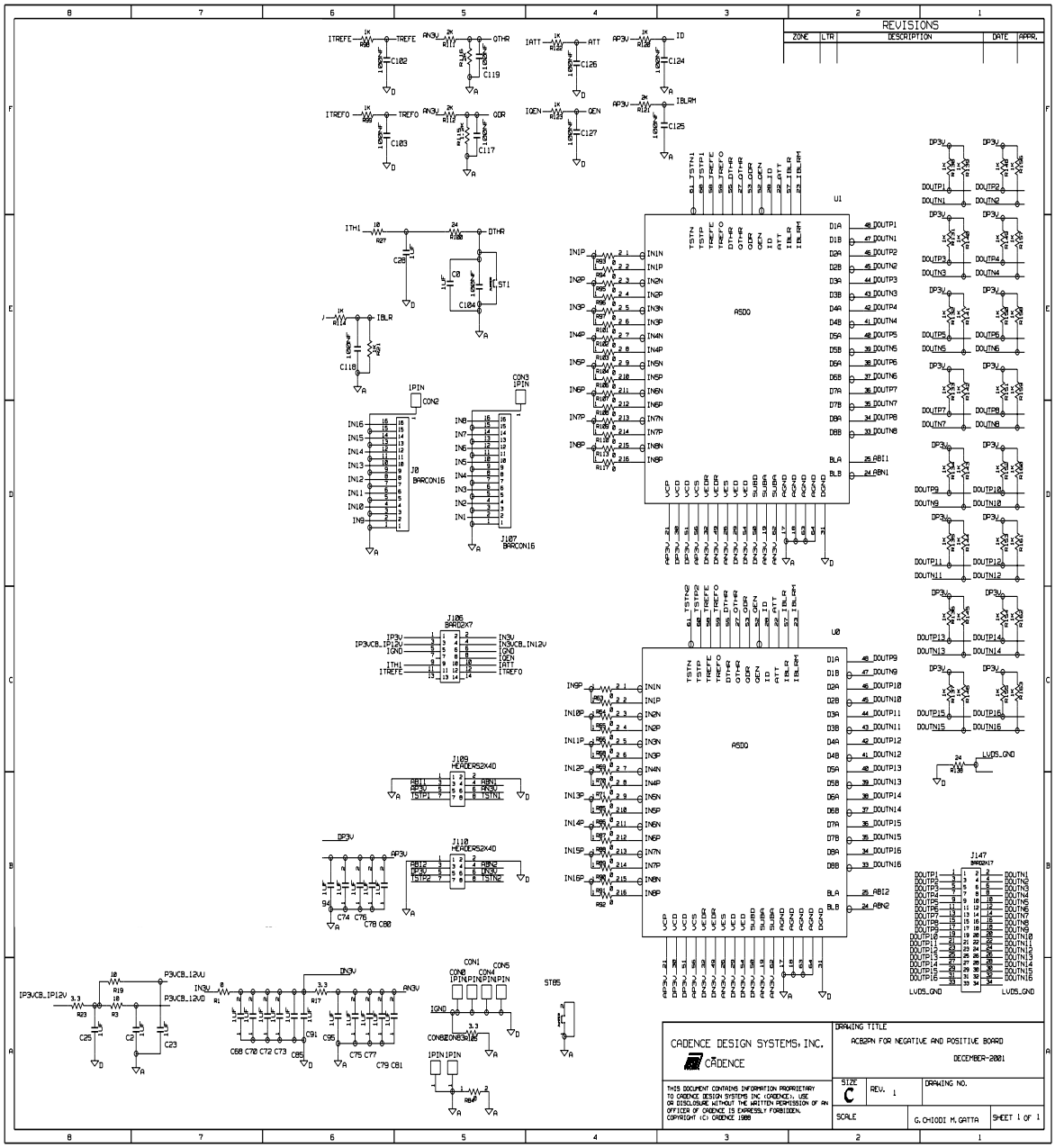


Fig.2. Schematics of the 16-channel ACB board. The schematic of the common base transistor as shown in Fig.1 has to be added to each input.

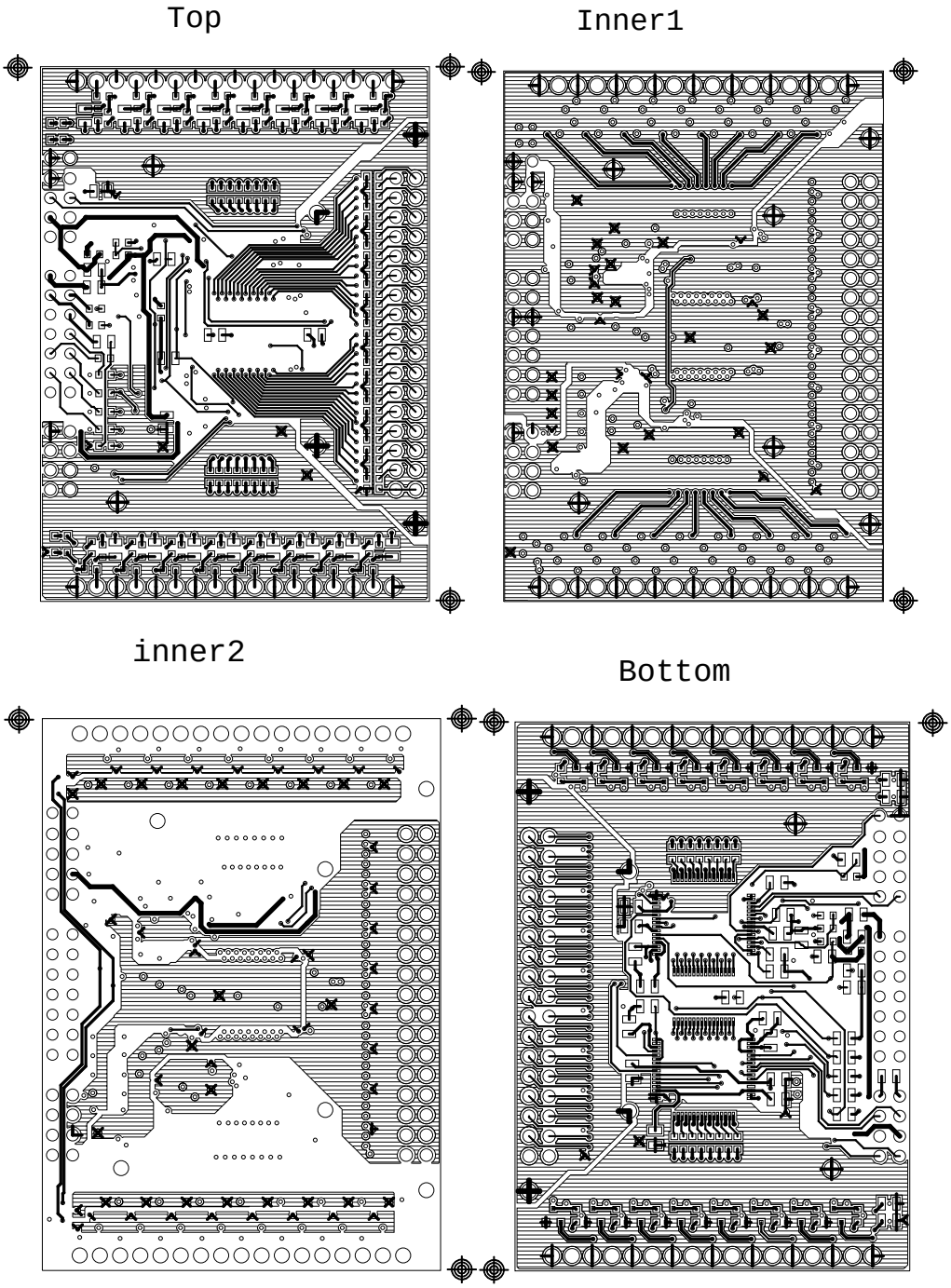


Fig.3. Layout of the 4-layer ACB board.

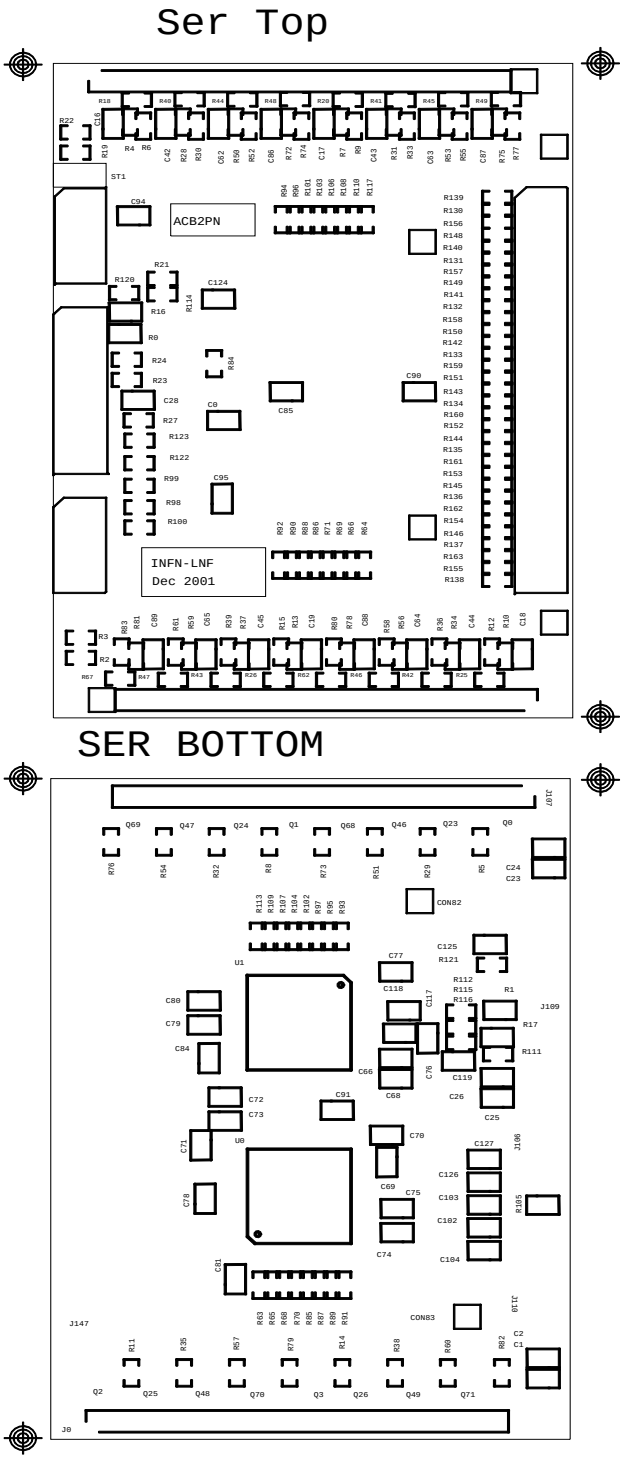


Fig.4. Assembling of the ACB board.

4 16-channel Spark Protection Board

The double stage resistor-diode circuitry is used in input of each channel, cf. Fig.5 and 6. In order to reduce the series noise, the first resistor is equal to 8.2Ω (SMD 2512, 1Watt) and the second one is 5Ω (SMD 1206, 10Ω in parallel, 0.25 Watt). The diodes are BAV99.

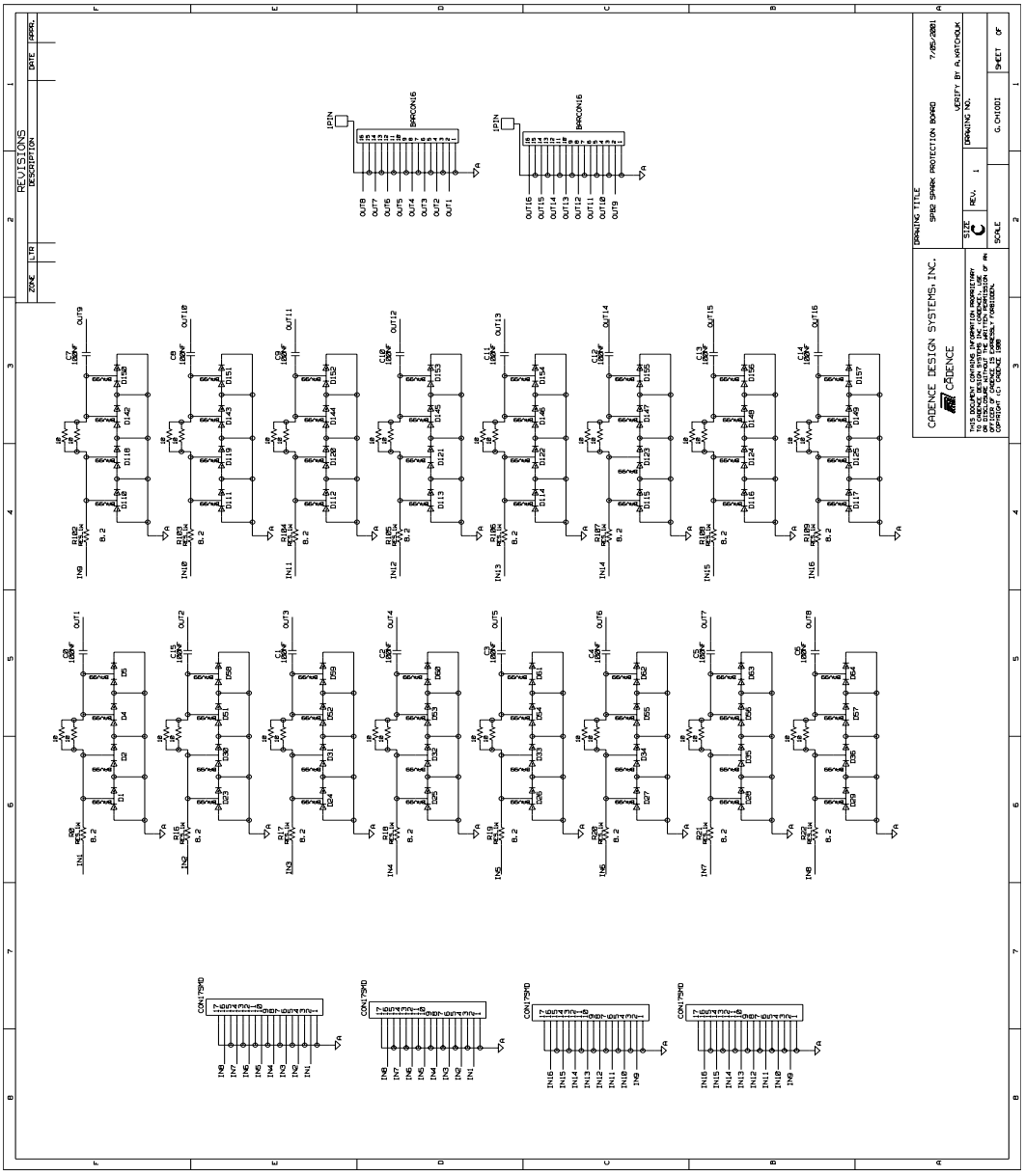


Fig.5. Schematics of the 16-channel SPB board.

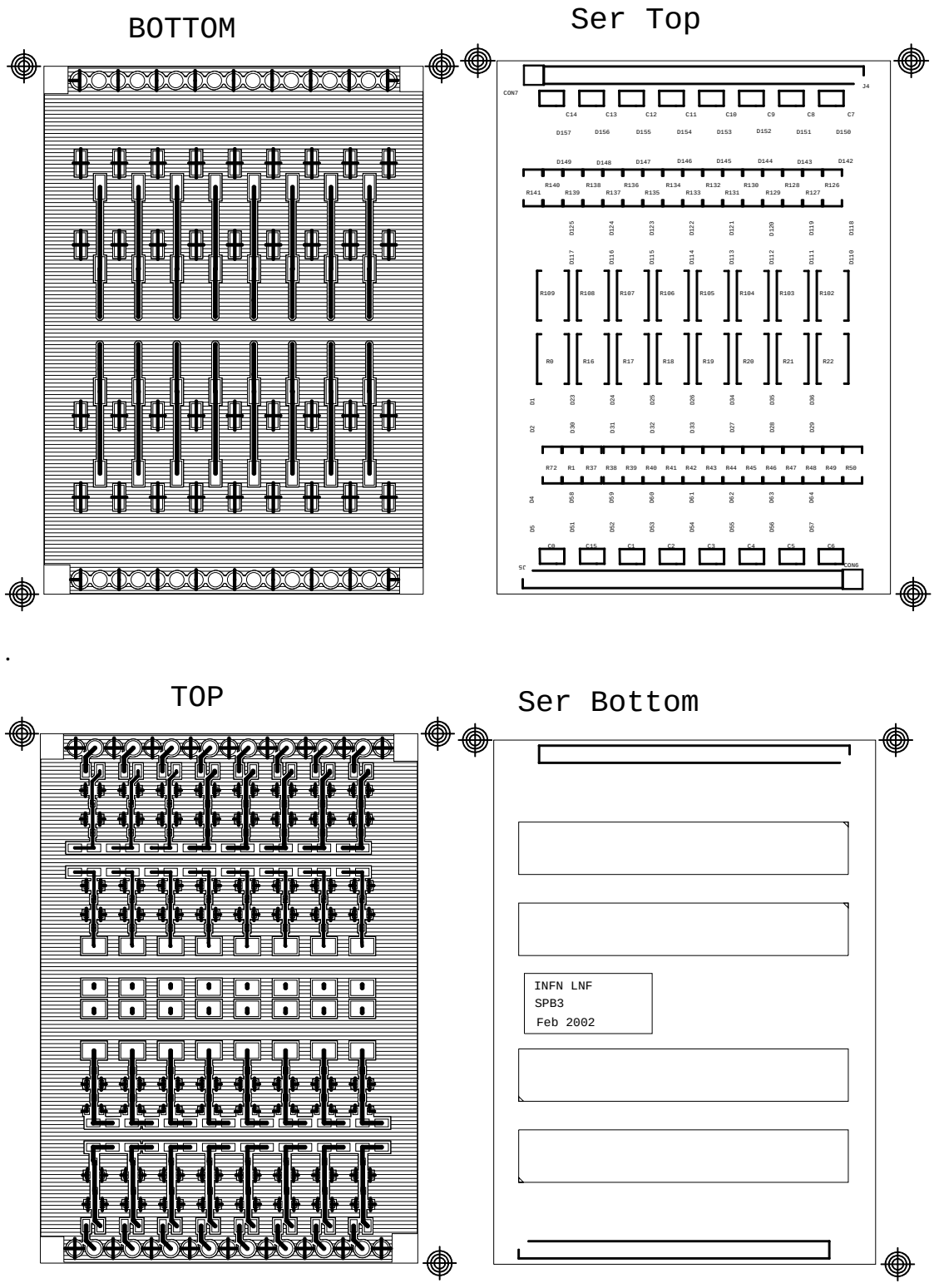


Fig.6. Layout of the 2-layer SPB board and its assembling.

5 Irradiation test

The components on the Spark Protection and ASDQ-chip boards were tested on radiation hardness using protons of 24 GeV/c. The post-radiation measurements indicate very satisfying operation of both boards (ACB and SPB) even after accumulating a dose of about 3 MRad and 1×10^{14} protons/cm^2.

Fig.7 illustrates, how the boards were located on the beam during irradiation.

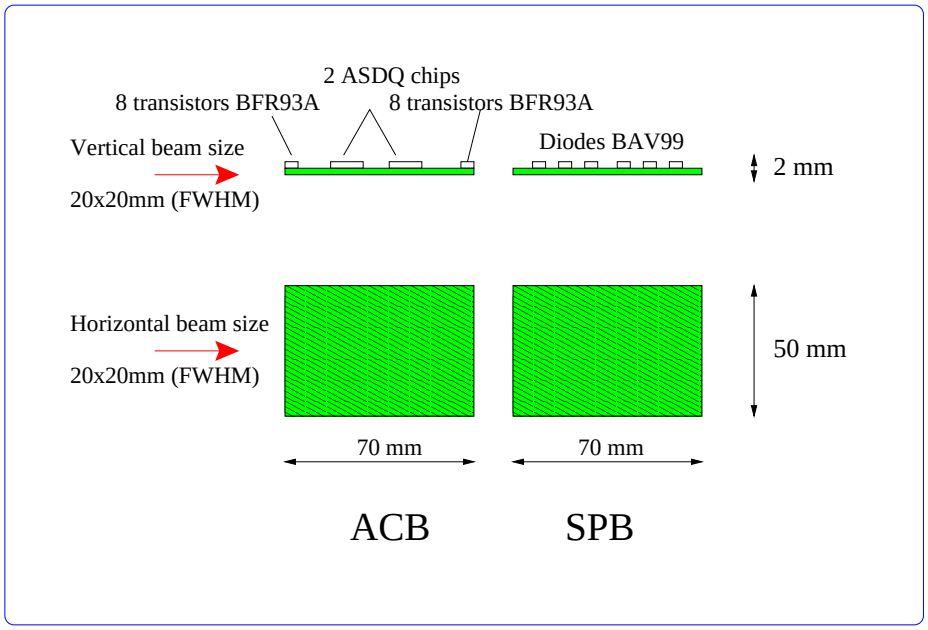


Fig.7. Position of the front-end boards ACB and SPB on the beam line.

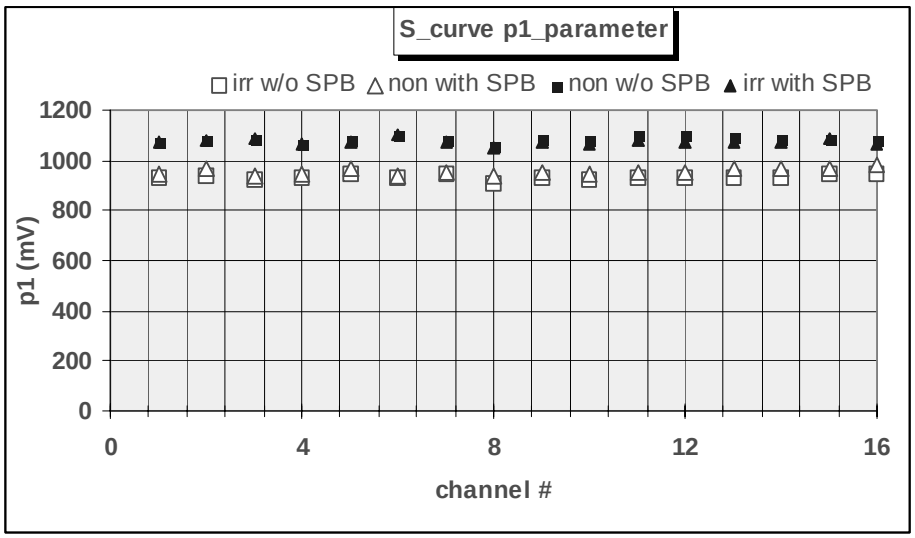
The ASDQ chips have got the full dose, as well as the central transistors and diodes. The peripheral transistors and diodes have got a much smaller dose due to the size of the proton beam (FWHM $\pm$ 20mm $\times$ 20mm).

In order to extract the effect of the irradiation, the S-curve method was used. A constant charge (40fC) was injected to the input of each channel and the threshold was scanned. Two fit parameters to the S-curve were determined: the mean value showing the sensitivity at the 50% efficiency level, and the root-mean square (RMS) of the distribution showing the noise.

The S-curve was measured before and after irradiation and the results are shown in Fig.8. The average of the mean value for 16 channels was measured to 1075mV before and 929.5mV after irradiation. One can conclude from this, that the sensitivity was reduced by 13.5%. Since there is no visible difference in sensitivity reduction between the channels, where the common base transistor was irradiated compared to those where it was not, we conclude that the reduction in sensitivity is

due to the ASDQ chip. The average RMS values of the distribution for the 16 channels were 19.8mV / 21.5mV before and 19.0mV / 26.3mV after irradiation (without/with SPB). Hence, the noise stayed practically within the same limits.

a)



b)

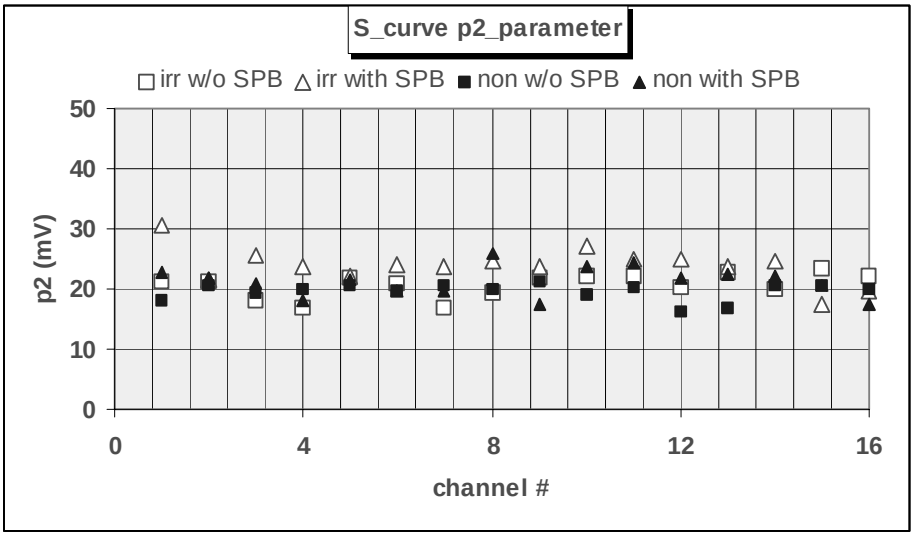


Fig.8. Results of measurements made for *a)* mean value (sensitivity, p1) and *b)* RMS (noise, p2). The parameters were determined for the case of ACB without and with SPB.

6 Summary

The schematics of both 16-channel Spark Protection Board (SPB) and 16-channel Amplifier Chip Board (ACB) based on ASDQ chip are presented. The boards are used to read out wire strips and cathode pads of the MWPC prototypes designed and tested for the Muon System of the LHCb experiment.

Some important characteristics of the front-end electronics based on ASDQ++ can be found in Ref.[3-5].

A common base transistor connected either to input *InA* of the ASDQ chip (in case of wire read-out) or *InB* (in case of cathode read-out) drastically improves the performance of the system, as discussed in Ref.[3]. The input impedance has been reduced by an order of magnitude and is constant in a wide frequency range (R_{in}*=25Ω at* I_E*=1 mA*). The detector capacitance has been extended by an order of magnitude with this configuration. Both features are achieved without disturbance of the main characteristics of the ASDQ chip, i.e. its high performance at high rates, excellent pulse shaping and other features.

The response of the ACB can be characterized by the peaking time of T_{peak}*≈8ns* and sensitivity of about *7mV/fC (at* C_{det}*=0).*

The ASDQ chip is radiation tolerant. The post-radiation measurements made at CERN indicate suitable operation of both boards up to doses of 3 *MRad* and 1×10^{14} *protons/cm*^{2} at *24GeV/c,* which is about 5 times more than expected for the Muon System in the places of highest irradiation after 10 years of LHCb operation.

The layout of the boards represent a general solution for the Muon System, i.e. the FE boards based on CARIOCA will be compatible to ACB and use the SPB as presented in this note.

Aknowlegements

The authors wish to acknowledge P.Campana, G.Martellotti, A.Lai and W.Riegler for support of this work and useful discussions. We also gratefully aknowlendge M.Glaser for his help during radiation test.

Appendix

ASDQ chip pin assignment

Pin		*Comment*
AGND	0V Analog	Analog Ground (reference)
SUBA	-3V Analog	Substrate Analog
VPP	Floating	Input protection
VCP	+3V Analog	Preamplifier Power Supply
VCS	+3V Analog	Shaper/BLR Power Supply
VES	-3V Analog	Shaper/BLR Power Supply
VCD	+3V Digital	Disc and Driver Power Supply
VED	-3V Digital	Discriminator Power Supply
SUBD	-3V Digital	Substrate Digital
VEDR	-3V Digital	Driver Power Supply
DGND	0V Digital	Digital Ground (reference)
TSTN	-0.2V to –0.8V	Negative going test strobe pulse
TSTP	-0.4V to –0.6V	Positive going test strobe pulse
TREFE	-3V to +1.5V	DC Test Voltage for even channels
TREFO	-3V to +1.5V	DC Test Voltage for odd channels
ATT	0V or +3V	Logical level to attenuate input by 2 (0V no attenuation)
DTHR	0V to +2V	Discriminator Threshold
OTHR	-3V to +3V	Trailing edge tracking control (-3V Analog in ACB)
IBLR	-3V to +3V	BLR current reference (+1.5V Analog or –0.7V Analog, see text)
IBLRM	2k to +3V	Channel 8 monitor current reference
QDR	-3V to +3V	dE/dx reference (-3V Analog in ACB)
QEN	0V or +3V	Logical level dE/dx enable (+3V dE/dx OFF)
ID	2k to +3V	Output current reference
BLA	Floating	Open collector (positive going channel 8 monitor output)
BLB	Floating	Open collector (negative going channel 8 monitor output)
InA		Negative going input (n=1-8)
InB		Positive going input (n=1-8)
DnA		Open collector output rising edge (n=1-8)
DnB		Open collector output falling edge (n=1-8)

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